(b) forming a piezoelectric thin film on top of the ground electrode, wherein the piezoelectric thin film varies in at least one characteristic across the wafer; and

(c) forming at least one upper electrode on top of the piezoelectric thin film,

wherein at least the ground electrode, the piezoelectric thin film and the at least one upper electrode form components, as a result of steps (a)-(c), in each of the plurality of acoustical wave devices, and

wherein at least one component in some of the plurality of acoustical wave devices is modified in its operational characteristic to compensate for the variation in the at least one characteristic of the piezoelectric thin film and is based on the location of the at least one acoustical wave device on the wafer.

25. (Once Amended) The wafer according to claim 24, wherein a length of the at least one upper electrode is dependent upon the intended position of the semiconductor substrate on the wafer.

26. (Once Amended) The wafer according to claim 24, wherein a width of the at least one upper electrode is dependent upon the intended position of the semiconductor substrate on the wafer.

27. (Once Amended) The wafer according to claim 24, wherein the step of forming at least one upper electrode forms a plurality of upper electrodes, and

wherein distances between each of the plurality of upper electrodes is dependent upon the intended position of the semiconductor substrate on the wafer.

C1 (cont

28. (Once Amended) The wafer according to claim 24, wherein said step (c) further includes a step,

(c1) connecting the at least one upper electrode to a bonding pad, and

wherein a shape of the bonding pad is dependent upon the intended position of the semiconductor substrate on the wafer.

29. (Once Amended) The wafer according to claim 28, wherein an area covered by the bonding pad is dependent upon the intended position of the semiconductor substrate on the wafer.

30. (Once Amended) The wafer according to claim 24, wherein said step (c) further includes steps,

(c1) connecting the at least one upper electrode to a bonding pad; and

(c2) connecting the at least one upper electrode and the

bonding pad to a connecting pattern,

wherein a shape of the connecting pattern is dependent upon the intended position of the semiconductor substrate on the wafer.

31. (Once Amended) The wafer according to claim 30, wherein a length of the connecting pattern is dependent upon the intended position of the semiconductor substrate on the wafer.

C1 Cont

32. (Once Amended) The wafer according to claim 30, wherein a width of the connecting pattern is dependent upon the intended position of the semiconductor substrate on the wafer.

33. (Once Amended) The wafer according to claim 24, wherein said step (c) further includes steps,

(c1) connecting the at least one upper electrode to a bonding pad; and

(c2) connecting the at least one upper electrode and the bonding pad to a connecting pattern,

wherein the connecting pattern is formed with an air bridge.

34. (Once Amended) The wafer according to claim 24, wherein the method according to which the device is manufactured includes a step,

(d) forming a capacitor on the same semiconductor substrate as the film acoustic wave device,

wherein a capacitance of the capacitor is dependent upon the intended position of the semiconductor substrate on the wafer.

35. (Once Amended) The wafer according to claim 24, wherein the semiconductor substrate is made of gallium arsenide (GaAs); the piezoelectric thin film is made of lead titanate ($PbTiO_3$); and the at least one upper electrode is a conductor substantially made of platinum (Pt).

C1 Cont

36. (Once Amended) The wafer according to claim 24, wherein the semiconductor substrate is made of silicon (Si); the piezoelectric thin film is made of lead titanate ($PbTiO_3$); and the at least one upper electrode is a conductor substantially made of Platinum (Pt).

37. (Once Amended) The wafer according to claim 24, wherein the piezoelectric thin film is made of PZT ($PbTiO_3$-$PbZrO_3$); and the at least one upper electrode and the ground electrode is a conductor substantially made of platinum (Pt).

38. (Once Amended) The wafer according to claim 24, wherein the piezoelectric thin film is made of zinc oxide (ZnO).

C1 (cont

39. (Once Amended) The wafer according to claim 24, wherein the piezoelectric thin film is made of aluminum nitride (AlN).

40. (Once Amended) The wafer according to claim 24, wherein an inductor is intended to be formed between the semiconductor substrate and the ground electrode.

Please add the following new claims:

C2

--61. The wafer of claim 24, wherein the varied characteristic of the piezoelectric thin film is thickness.

62. The wafer of claim 24, wherein the piezoelectric thin film is thicker in the middle of the wafer and becomes thinner as it extends out towards the periphery of the wafer.--

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